**WHAT IS CLAIMED IS:**

1. In a receiver that includes a clock recovery circuit for extracting a recovered clock signal from an incoming data signal, a loss-of-signal detector comprising:

a delay circuit coupled to receive the incoming data signal and configured to shift a phase of the incoming data signal by a predetermined delay $\Delta T$ to generate a delayed data signal;

a flip-flop coupled to receive the recovered clock signal at one input and the delayed data signal at a clock input;

an integrator coupled to an output of the flip-flop;

a switch coupled to the integrator and configured to reset the integrator; and

a comparator having a first input coupled to an output of the integrator and a second input coupled to a threshold voltage,

wherein, the delay circuit is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal.

2. The loss-of-signal detector of claim 2 wherein the flip-flop is configured to generate an error signal when a transition of the delayed data signal falls outside of the range $(T/2)\pm\Delta T$, where T is the period of the recovered clock signal.

3. The loss-of-signal detector of claim 2 wherein the predetermined delay $\Delta T$ is substantially equal to about 1/4 of the recovered clock signal period T.

4. The loss-of-signal detector of claim 1 wherein the delay circuit comprises a buffer implemented in current-controlled complementary metal-oxide-semiconductor ($C^3MOS$) logic.

5. The loss-of-signal detector of claim 4 wherein the flip-flop is implemented in $C^3MOS$ logic.

6. The loss-of-signal detector of claim 2 wherein the integrator is configured to integrate a plurality of error signals generated by the flip-flop for an integration period τint, and to generate a bit error rate signal $V_{BER}$.

7. The loss-of-signal detector of claim 6 wherein the integrator comprises:

a current source configured to supply current $I_0$;

a capacitor; and

a first switch coupled between the current source and the capacitor, and configured to open or close in response to the error signal generated by the flip-flop.

8. The loss-of-signal detector of claim 7 wherein the integrator further comprises a second switch coupled in parallel to the capacitor and configured to discharge the capacitor in response at the end of each integration period τint.

9. The loss-of-signal detector of claim 6 wherein the comparator compares $V_{BER}$ to a threshold level and generates a loss-of-signal indicator when $V_{BER}$ exceeds the threshold level.

10. The loss-of-signal detector of claim 9 wherein the comparator comprises a hysteresis whereby the loss-of-signal indicator is asserted when $V_{BER}$ exceeds a first threshold Vt1, and is not cleared until $V_{BER}$ drops below a second threshold Vt2 that is lower than the first threshold Vt1.

11. The loss-of-signal detector of claim 7 wherein the first switch of the integrator comprises a pair of differentially coupled metal-oxide-semiconductor field effect transistors (MOSFETs).

12. The loss-of-signal detector of claim 11 wherein the pair of MOSFET are of p-channel type.

13. The loss-of-signal detector of claim 11 wherein the integrator further comprises a unity-gain buffer coupled between the pair of differentially coupled MOSFETs.

14. The loss-of-signal detector of claim 8 further comprises a divider circuit coupled to receive the recovered clock signal and configured to generate a signal representing the integration period τint.

15. A high speed receiver comprising:

a clock and data recovery block coupled to receive an incoming data signal and configured to extract a recovered clock signal from the incoming data signal;

a retiming circuit coupled to receive the incoming data and the recovered clock signal and configured to generate a retimed data signal for further processing; and

a statistical loss-of-signal (SLOS) detector coupled to receive the recoverèd clock signal and the incoming data signal, and configured to measure a bit error rate of the incoming data signal and to detect a loss-of-signal condition,

wherein the SLOS detector is configured such that it adds as capacitive loading a single flip-flop to the recovered clock signal and a single delay circuit to the incoming data signal.

16. The high speed receiver of claim 15 wherein the single delay circuit delays the incoming data by a predetermined window ΔT to generate a delayed data signal, and

wherein, the single flip-flop is configured to generate an error signal when a transition of the delayed data signal falls outside of the range $(T/2)\pm\Delta T$, where T is the period of the recovered clock signal.

17. The high speed receiver of claim 16 wherein the predetermined window ΔT is substantially equal to about ¼ of the period T of the recovered clock signal.

18. The high speed receiver of claim 16 wherein the SLOS detector further comprises:

an integrator coupled to the single flip-flop and configured to integrate a plurality of error signals over an integration period τint to generate a signal $V_{BER}$ that provides a measure the bit error rate of the incoming data.

19. The high speed receiver of claim 18 wherein the integrator comprises a switch that couples a current source to a capacitor in response to the error signal generated by the single flip-flop.

20. In a receiver that includes a clock recovery circuit for extracting a recovered clock signal from an incoming data signal, a method for detecting statistical loss of signal, the method comprising:

delaying the incoming data signal by a window ΔT that is symmetrical relative to the recovered clock signal;

latching the recovered clock signal using the delayed data signal as clock to generate an error signal, wherein a single latch generates the error signal

whenever a transition of the delayed data signal falls outside of the range (T/2)±ΔT, where T is the period of the recovered clock signal;

integrating a plurality of error signals over a predetermined period of time $\tau$int to arrive at a bit error rate of the incoming data signal; and

comparing the bit error rate with a predetermined threshold to detect a loss-of-signal condition.

21. The method of claim 20 wherein the step of delaying delays the incoming data signal by ¼ of the period T of the recovered clock signal.